R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR AMENDMENTS TO THE CLAIMS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 2 and 6 and in the specification as originally filed, for example, on page 28, line 14, through page 29, line 15. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-6, 8, 11, 14-20 and 22 under 35 U.S.C. §102 as being anticipated by Stiffler (U.S. Patent No. 4,736,376) is respectfully traversed and should be withdrawn.

Stiffler is directed to a self-checking error correcting encoder/decoder (Title).

In contrast to Stiffler, the presently claimed invention (claim 1) provides (i) a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal, (ii) a bypass circuit configured to generate a second syndrome signal in response to the first syndrome signal and a bypass signal, and (iii) a second circuit configured to (i) detect an error when bits of the second syndrome signal are not all

the same state and (ii) generate an error location signal in response to the second syndrome signal, where the error location signal (i) is generated in response to fewer than all of the bits of the second syndrome signal and (ii) describes a location of a single bit error detected in the read data and parity signals. Claims 14, 15 and 22 include similar limitations. Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, the two sets of signals [c1...c4] correspond to the presently claimed first syndrome signal and the signals [g1...g4] correspond to the presently claimed bypass signal (as suggested on page 3, lines 14-21 and on page 4, lines 4-5 of the Office Action and for which Applicants' representative does not necessarily agree), Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims.

It appears that the Examiner interprets the two sets of signals [c1...c4] of Stiffler as being a first syndrome signal merely because the signals are shown presented by the **1st stage** syndrome generator (430) in FIG. 4 of Stiffler. Furthermore, it appears that the Examiner interprets the signals [g1...g4] of Stiffler as being a bypass signal merely because no other signal is

presented to the 2nd stage syndrome generators (442 and 444) in addition to the signals [c1...c4]. However, Stiffler does not support the interpretation presented in the Office Action. Specifically, Stiffler explicitly provides that the signals [c1...c4] and the signals [g1...g4] are computed parity relationships and nyble parities, respectively, which are **used to generate syndrome bits.** Stiffler states:

> **Each circuit half combines the results of the four parity relationships computed from the data bits available to it with the four nyble parities computed by the other half circuit to generate four syndrome bits** (half of the total eight-bit syndrome). This combination is performed in second stage syndrome generators 442 and 444. Generator 442 receives **four bits, c1-c4, corresponding to the four computed parity relationships calculated from the input data bits** via bus 438 and **four nyble parities, g1-g4**, received from the other circuit half over terminal 441 and bus 440. Similarly generator 444 receives the complemented parity relationship bits, e1-e4, from generator 430 over bus 437 and the nyble parity bits g1-g4 from the other decoder half. Generator 442 generates four syndrome bits, h1-h4, on bus 456 and generator 444 generates four bits, i1-i4, which are the complements of the bits generated by generator 442. The complemented bits are provided on bus 454 to be used in a later stage of processing (column 8, line 63-column 9, line 13 of Stiffler, emphasis added).

Since (i) the two sets of signals [c1...c4] are computed parity relationships rather than a syndrome signal, (ii) the signals [g1...g4] are nyble parities rather than a bypass signal as presently claimed and (iii) the second stage syndrome generators

442 and 444 combine the four parity relationships with the four nyble parities to generate four syndrome bits, it follows that Stiffler does not disclose or suggest (i) a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal AND (ii) a bypass circuit configured to generate a second syndrome signal in response to the first syndrome signal and a bypass signal, as presently claimed. Therefore, Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, the statement in lines 5-7 on page 4 of the Office Action that "the 2nd Stage Syndrome Generators 442 and 444 [of Stiffler] are bypassed during encoding, hence are responsive to **the** bypass signal generated by Encoder/Decoder Control 420" does not appear to be technically correct. Specifically, the signals [h1...h4] and [i1...i4] generated by the second stage syndrome generators are presented to the encoder 464 of Stiffler for use in generating the parity code word (i.e., the two sets of signals [s1...s4]) to be appended to the data before the data is stored (see column 10, lines 4-13 of Stiffler). Thus, contrary to the position taken in the Office Action, the 2nd Stage Syndrome Generators 442 and 444 are used during encoding.

Furthermore, Stiffler appears silent regarding the Encoder/Decoder Control 420 generating a bypass signal. Indeed, the Office Action previously stated that the signals [g1...g4], which are not generated by the Encoder/Decoder Control 420, were considered to correspond to the presently claimed bypass signal. Thus, the office Action fails to factually support a *prima facie* case that Stiffler discloses or suggests each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, the signals [j1...j4] of Stiffler correspond to the presently claimed error location signal (as suggested on page 4, lines 7-21 of the Office Action and for which Applicants' representative does not necessarily agree), Stiffler does not disclose or suggest an error location signal that describes a location of a single bit error detected in the **read data AND parity signals**, as presently claimed. Therefore, Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, Stiffler states:

> One set of output signals, j1-j4, indicate the position of a potentially erroneous bit. However, since the half circuit does not have the complete syndrome information at this

> stage, **the signals j1-j4 cannot specify the exact position of the erroneous bit**. Instead, the signals j1-j4 indicate the modulo-4 position of a potentially erroneous bit. Specifically, if bit j1 is a logical "1", then a bit in one of the bit positions 4i+1, i=0,1,2,3 may be in error; if bit j2=" 1" then one of bits 4i+2, i=0,1,2,3 may be in error (column 9, lines 28-37 of Stiffler).

Since the signals [j1...j4] of Stiffler cannot specify the exact position of the erroneous bit, it follows that the signals [j1...j4] of Stiffler do not describe a location of a single bit error detected in the **read data AND parity signals**, as presently claimed.

Furthermore, Stiffler does not disclose or suggest using the signals [j1...j4] to describe a location of a single bit error detected in the **read data AND parity signals**, as presently claimed. Specifically, the signals [j1...j4] are combined with signals [m1...m4] by the second stage syndrome decoder 484 to generate bit pointers [n1...n16] which identify only the position of an erroneous **data** bit (see FIG. 4 and column 9, lines 56-66 of Stiffler). Stiffler appears silent regarding the signals [j1...j4] or [n1...n16] also describing a location of a single bit error detected in the **parity signals**, as presently claimed. Therefore, Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-13, 16-21 and 23 depend, either directly or indirectly, from either claim 1, claim 15 or claim 22 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 7, 9, 10, 12, 13, 21 and 23 under 35 U.S.C. §103(a) as being unpatentable over Stiffler is respectfully traversed and should be withdrawn.

Claims 7, 9, 10, 12, 13, 21 and 23 depend, either directly or indirectly, from either claim 1 or claim 22 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, with respect to claim 7, the Office Action fails to present factual evidence or sufficient reasoning to support the position that:

> Figure 4 of Stiffler is a block diagram for establishing the logical layout of the design and that the actual circuit layout is based on obvious engineering design choices, hence an embodiment of the design in the Stiffler patent including 2nd Stage Syndrome Generator 444 in Figure 4 as part of the second circuit, 1st Stage Syndrome Decoder 458, is an obvious engineering design choice based on actual design requirements such as cost feasibility, available space, stray capacitance, etc. (page

16, last 5 lines through page 17, line 2 of the Office Action).

Applicants' representative respectfully requests that the Examiner provide factual proof or an affidavit under 37 C.F.R. §1.104(d)(2) to substantiate the conclusion of obvious engineering design choice presented on pages 16 and 17 of the Office Action or withdraw the rejection.

With respect to claims 9 and 23, the Office Action fails to factually support a *prima facie* case of obviousness (M.P.E.P. §2142). Assuming *arguendo*, the signals I1-I4 are similar to the presently claimed inverse of the second syndrome signal, Stiffler does not teach or suggest each and every element of the presently pending claims 9 and 23. Specifically, Stiffler fails to teach or suggest one or more OR gates configured to receive an inverse of said second syndrome signal and present the error detected signal, as presently claimed. In particular, the Office Action points to gates 930, 936, 942 and 948 in FIG. 9 of Stiffler. However, gates 930, 936, 942 and 948 of Stiffler do not receive the signals I1-I4. Therefore, Stiffler does not teach or suggest each and every element of the presently pending claims 9 and 23. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Stiffler does not teach or suggest one or more exclusive OR gates configured to receive an inverse of said second syndrome signal and present an intermediate signal, as

presently claimed. Specifically, the Office Action points to gates 1202-1208 in FIG. 12 of Stiffler as corresponding to the presently claimed one or more exclusive OR gates. However, the gates 1202-1208 of Stiffler are part of the encoder 464 in FIG. 4 of Stiffler. The gates 1202-1208 are configured to generate parity bits [S1...S4]. The Office Action presents no objective evidence or a convincing line of reasoning why one skilled in the art would consider the parity bits [S1...S4] of Stiffler to necessarily be the same as the presently claimed intermediate signal. Therefore, the Office Action fails to factually support a *prima facie* conclusion of obviousness and the rejection should be withdrawn (M.P.E.P. §2143).

Furthermore, the Office Action fails to present objective evidence or a convincing line of reasoning to support the Examiner's assertion that:

> . . . NAND gates 902-918 in Figure 9 substantially invert output, which is equivalent to ORing the inverse of the inputs; hence use of an inverted intermediate signal is substantially an equivalent embodiment. One of ordinary skill in the art at the time the invention was made would have been highly motivated to invert the intermediate signal based on obvious engineering design choices such as available circuitry, design layout, and intrinsic qualities of circuit components that effect overall efficiency and cost of circuitry. (Page 19, lines 1-7 of the Office Action.)

Applicants' representative respectfully request that the Examiner provide factual proof or an affidavit under 37 C.F.R. §1.104(d)(2)

to substantiate the conclusion of obvious engineering design choice presented on page 19 of the Office Action or withdrawn the rejection of claims 9 and 23.

With respect to claim 12, the Office Action fails to specifically point out which signal generated by the encoder/decoder control 420 is considered to be similar to the presently claimed bypass signal. Assuming, *arguendo*, the second stage syndrome generators 442 and 444 could be considered by one of skill in the art to be similar to the presently claimed bypass circuit, neither circuit 442 nor the circuit 444 of Stiffler receive a signal from the encoder/decoder control circuit 420 (see FIG. 4 of Stiffler). Furthermore, assuming, *arguendo*, one of skill in the art would consider the signals [c1...c4] to be similar to the presently claimed first syndrome signal and the signals [h1...h4] to be similar to the presently claimed second syndrome signal, the assertion in the Office Action that the signals [h1...h4] are a **modified version** of the signals [c1...c4] clearly shows that Stiffler does not teach or suggest a bypass circuit configured to present a first syndrome signal **as** the second syndrome signal. The position taken in the Office Action that the signals [c1...c4] are "substantially" presented as the signals [h1...h4] does not appear to address the specific limitations of claim 12. In particular, nowhere in claim 12 is it stated that the

first syndrome signal is "substantially" presented as the second syndrome signal.

Furthermore, the Office Action admits that Stiffler does not explicitly teach an apparatus bypass circuit comprising one or more logic gates configured to receive the bypass signal as presently claimed (see page 20, lines 17-18 of the Office Action). Furthermore, the assertion by the Examiner that the "2nd Stage Syndrome Generators 442 and 444 . . . in FIG. 4 of Stiffler are required to operate to transfer output data in two different modes" and "hence although Stiffler does not explicitly teach that the 2nd Stage Syndrome Generators 442 and 444 receive **the bypass signal** from Encoder/Decoder 420" assumes the existence of a bypass signal. Furthermore, if the Examiner's analysis is correct that the circuits are required to operate in the manner asserted, Stiffler does not appear to be enabling since Stiffler does not teach the necessary signals.

Furthermore, the Office Action's assertion that one of ordinary skill in the art at the time of the invention would have recognized the **need** for notifying the second stage syndrome generators 442 and 444 in order to implement the design in the Stiffler patent (page 21, lines 1-5 of the Office Action) appears to indicate that the Stiffler does not disclose a necessary signal. Furthermore, the statement in the Office Action that one of ordinary skill in the art would have modified the teachings of the

Stiffler patent by including use of an apparatus bypass circuit comprising one or more logic gates configured to receive the bypass signal because one of ordinary skill in the art would have recognized that the use of a bypass circuit would have provided the opportunity to implement the design in the Stiffler patent appears to clearly acknowledge that the Stiffler patent does not teach or suggest a bypass circuit as presently claimed.

With respect to claim 13, the position taken in the Office Action that FIG. 8 of Stiffler substantially teaches one or more logic gates are selected from the group consisting of AND, NAND, NOR and OR gates is not correct. Specifically, referring to FIG. 8 of Stiffler, one skilled in the art would clearly recognize that the gates shown are exclusive OR gates. One skilled in the art would not consider exclusive OR gates part of the group consisting of AND, NAND, NOR and OR gates. As such, the rejection of claim 13 is not proper and should be withdrawn.

With respect to claim 21, the position taken in the last two lines of page 21 and lines 1-5 on page 22 of the Office Action that Stiffler substantially teaches the bypass circuit is configured to present all of the bits of the second syndrome signal having the same state in response to the bypass signal having the second state because if no errors occur the second syndrome signal is equal to zero does not present a proper *prima facie* case of obviousness (21 M.P.E.P.§2143). Specifically, the Office Action

fails to point to the specific signal from the Encoder/Decoder Control 420 that is considered to be the bypass signal. Furthermore, despite the position taken in the Office Action, the syndrome signal being equal to zero if no errors occur merely suggests that the bits of the syndrome signal are set to the same state in response to the data signal rather than in response to a second state of the bypass signal, as presently claimed. Therefore, Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently pending claim 21 is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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